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OPTIMIZATION DESIGN OF LOW POWER FLIPFLOP USING CONDITIONAL PULSE ENHANCEMENT METHOD

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ABSTRACT

Design a low-power pulse-triggered flip-flop (FF) using conditional pulse enhancement method. An AND function for the pulse generation control logic which is removed from the critical path to provide a faster discharge operation. A simple two transistor AND gate design is used to reduce the circuit complexity. A conditional pulse enhancement technique is to speed up the discharge along the critical path only when needed. The transistor sizes in delay inverter and pulse generation circuit can be reduced for power saving. Various post layout simulation results based on nanometer technology. The design features that the best power-delay product performance in existing designs under comparison. The maximum power saving against existing designs is up to 38.4%. The average leakage power consumption is reduced by a factor of 3.52

Keywords—Flip-flop, low power, pulse-triggered

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power [1]. Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave-based FF in the applications of high-speed operations [2]–[5]. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less

sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulsewidth control in the face of process variation and the configuration of pulse clock distribution network [4].

Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [6]. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse.

II. EXISISTED IMPLICIT-TYPE P-FF DESIGN WITH PULSE CONTROL SCHEME

A. Implicit Pulsed DCO Flipflop

Implicit pulse triggered data close to output (ip-DCO) fig 2.1 [6]-[14] contains an AND logic based pulse generator and a semi dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node controls two larger MOS transistors (P2 and N5). The large capacitive load to node causes speed and power performance degradation.

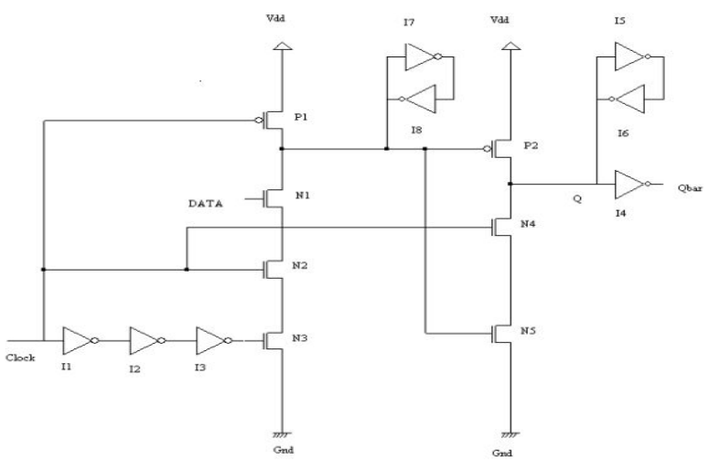


Figure 2.1 IP-DCO Flip-flops

Considering the pulse-triggered flipflop has a negative setup time and the clock arrives earlier than the input signals so that to place the pulse part closet to GND. So, the internal node Z can be pre-discharged before the input signals come. Therefore, the discharge process of node X or Q can be fast which results in more negative setup time and improving the performance of the designed flipflop. Negative setup time provides soft clock edge property, which is powerful in eliminating clock skew and jitter from timing budget in critical paths.

B. Modified Hybrid Latch Flipflop

Modified Hybrid Latch Flip Flop (MHLFF) fig 2.2 [6]-[14] is employing a static latch structure in which the node is no longer precharged periodically by the clock signal. A weak pull up transistor P1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero. This design eliminates the unnecessary discharging problem at node Q but it encounters a longer D-to-Q delay during 0 to 1 transitions because node is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node X becomes floating when output and input data both equal to 1.

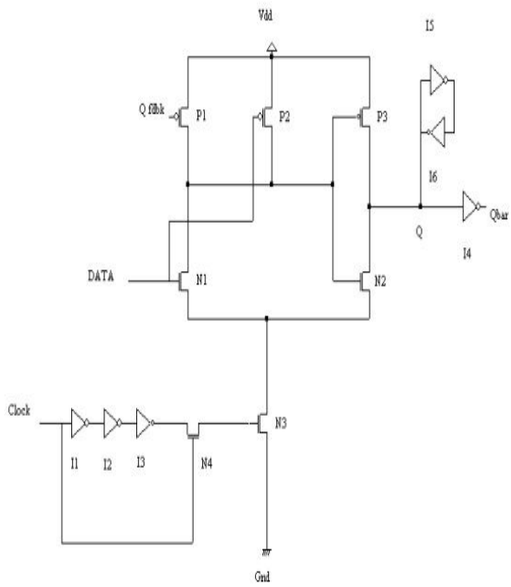


Figure 2.2 Modified Hybrid Latch Flip Flop

Extra DC power emerges if node X is drifted from an intact 1. MHLFF samples the data on one edge of the clock and eliminates the obstruction (delay) of data flow on the reverse edge. HLFF is mainly aimed to design the substantial reduction in latch latency and clock load.

The basic operation is similar to latch because it delivers a soft clock edge which allows for the stack passing and minimizing the effects of clock skew on cycle time. This cycle time is determined by an assimilated one-shot derived from the clock edge. Figure 6.4 shows the basic construction of MHLFF. Before the rising edge of the clock, the node X precharged to VDD and node Q holds the previous data, since the transistor N1 and N4 are off while N3, N6, and P1 are on. At the rising edge of the clock, the transistor N1 and N4 turn on while N3 and N6 stay on for three inverter delays. During this period the flip-flop is transparent and the data is sampled into the latch. When the transition of CKDB is low, the node X is decoupled from D, either it stays in that logic or begins to precharge to VDD by P3. The node X is completely precharged to hold the value of X to VDD at the negative edge of the clock.

C. Single Ended Conditional Capture Energy Recovery Ff

Single ended Conditional Capture Energy Recovery (SCCER) fig 2.3 Flipflop using a conditional discharge technique is used in which the keeper logic in ip-DCO replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node. The discharge path contains nMOS transistors N2 and N1connected in series. In order to eliminate superfluous switching at node, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high.

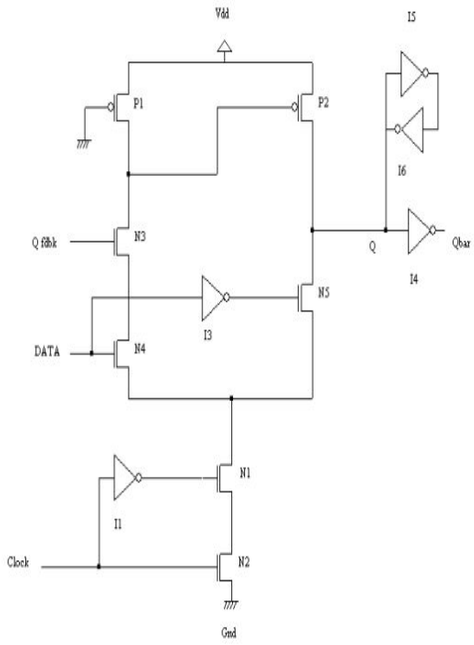


Figure 2.3 Single ended Conditional Capture Energy Recovery Flip Flop

The worst case timing of this design occurs when input data is 1 and node is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull-up transistor P1. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

SCCER is a single-ended version of the DCCER flipflop. The transistor N3, controlled by the output Q_fdbk, provides conditional capturing. The right-hand side evaluation path is static and does not require conditional capturing. Placing N3 above N4 in the stack reduces the charge sharing.

III. SCHEMATIC AND LAYOUT OF EXISTING FLIP-FLOP DESIGNS

A. Ip-Dco Ff Schematic Design

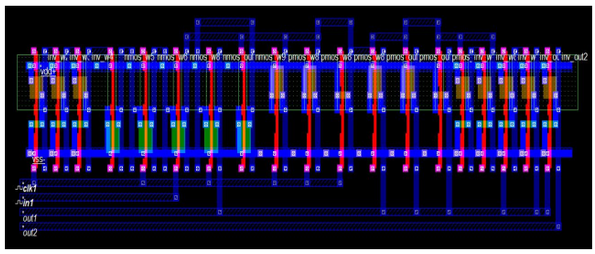


Figure 3.1 Layout Design of IP-DCOFF

B. MHLLFF Schematic Design

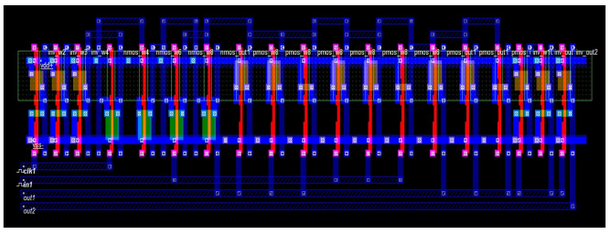


Figure 3.2 Layout Design of MHLLFF

C. SCCERFF - Schematic Design

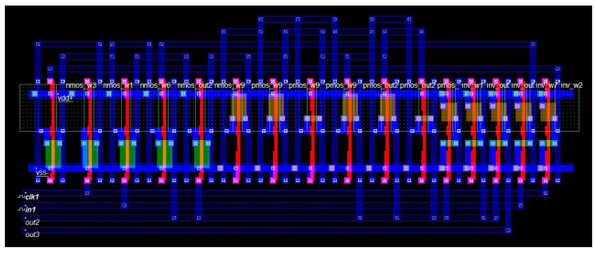
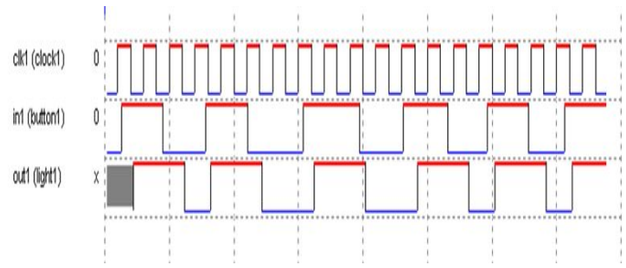


Figure 3.3 Layout Design of SCCERFF

IV. SIMULATION RESULTS



(a)

Schematic design output

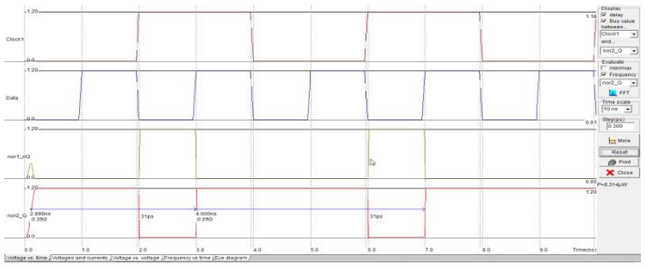


Figure 4.1(a),(b) Voltage vs. time characteristics

V. PROPOSED ENHANCED P-FLIPFLOP

A. EPTFF - Schematic Design

Fig 6.1 In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normally turned off because output node is pulled high most of the time. It steps in when output node is discharged to V_{tp} below $V_{dd.}$ The generated pulse is taller, which enhances the pull-down strength of transistor N1. After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path. The voltage level of Node X rises and turns off transistor P3 eventually. With the intervention of P3, the width of the generated discharging pulse is stretched out. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1.

The leads to a better power performance than those schemes using an indiscriminate pulse width enhancement approach. Another benefit of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunken transistors in the critical discharging path and in the delay inverter.

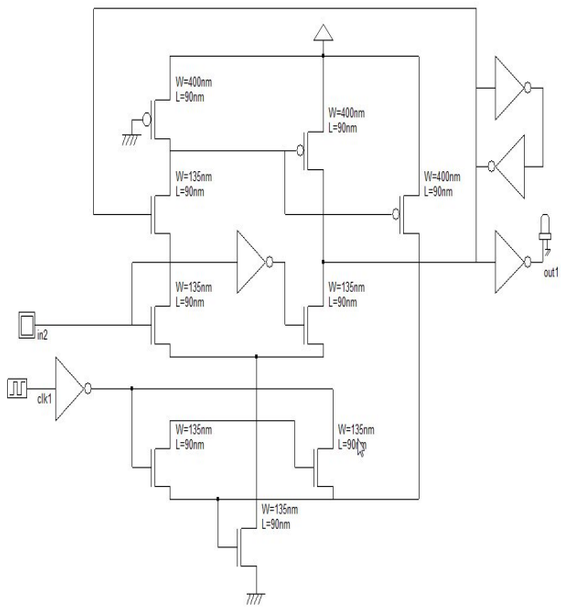


Figure 5.1 Schematic design of EPTFF

VI. LAYOUT DESIGN OF PROPOSED FLIPFLOP

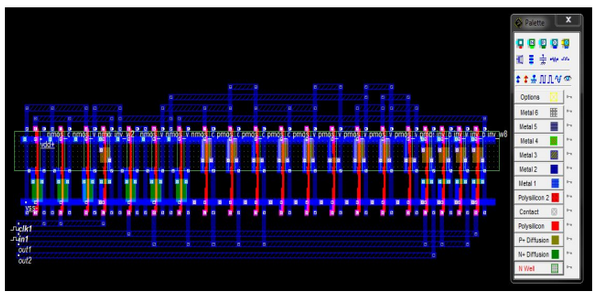


Figure 6.1 Layout Design of EPTFF

VII. SIMULATION SETUP

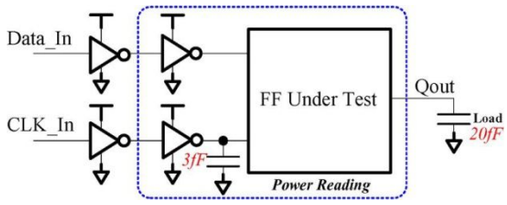


Figure 7.1 Simulation Setup

The operating condition used in simulations is 500 MHz/1.0V. Since pulse width design is crucial to the correctness of data capturing as well as the power consumption, the pulse generator logic in all designs are first sized to function properly across process variation. All designs are further optimized subject to the tradeoffs between power and D-to-Q delay, i.e., minimizing the product of the two terms. The simulation setup model is to mimic the signal rise and fall time delays, input signals are generated through buffers. Considering the loading effect of the FF to the previous stage and the clock tree, the power consumption's of the clock and data buffers are also included. The output of the FF is loaded with a 20-fF capacitor. An extra capacitance of 3 fF is also placed after the clock buffer in fig 7.1. Due to the extra voltage boost from transistor P3, pulses generated to capture input data "1" are significantly enhanced in their heights and widths compared with the pulses generated for capturing data "0". The changes in the width and the height of the generated discharge pulses under different process corners. Although significant fluctuations in pulse width and height are observed, the unique conditional pulse enhancement scheme works well in all. The power consumption of the enhanced pulse triggered lop design is the lowest in all test patterns due to a shorter discharging path.

VIII. AREA MEASUREMENT

A.Manual Method

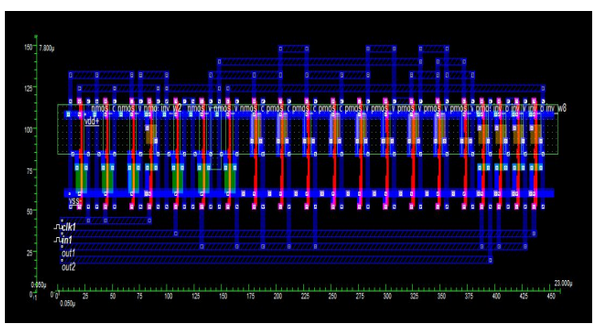


Figure 8.1 Area measurements by Manual method

B. Property Method

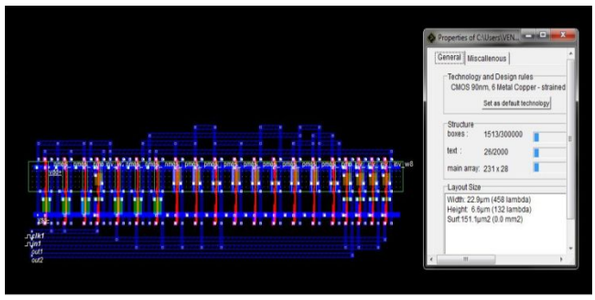


Figure 8.2 Area measurements by Property method

C. Power Measurements

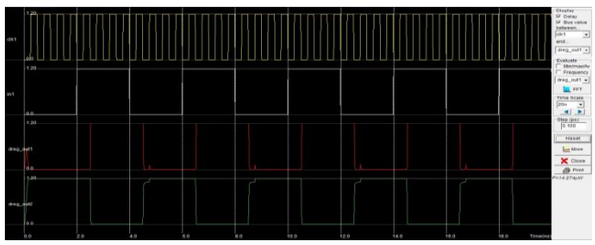


Figure 8.3 Voltage vs Time

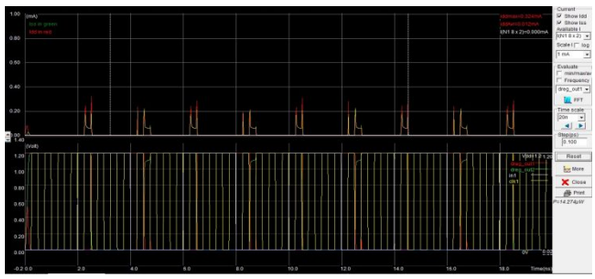


Figure 8.4 Voltage vs Current

IX. COMPARISON OF PROPOSED AND EXISTING METHOD

Low Power Flipflops	Average Power(µW)	Surface Area(µm^2)
MHLL Flipflop	33.914	194.6
IPDCO Flipflop	21.433	203.6
SCCER Flipflop	19.817	179.8
Proposed PFF	**14.274**	**151.4**

Table 9. Comparison of power and area

X. CONCLUSION

Low power pulse triggered flipflop design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum.

The various flip-flop designs like ip-DCO, MHLLF and SCCER are designed in Microwind DSCH tool and those result waveforms are analyzed and discussed. Simulation results indicate that the proposed design excels rival designs in performance indexes such as power, delay and power delay product PDP. The voltage vs time and voltage vs frequency characteristics of the enhanced pulse triggered flipflop design are discussed

In order to compare the layout area of the Enhanced pulse triggered flipflop with the existing designs, The Export Microwind tool to be used and generate the layout and area analysis of the flipflop can be performed. This proposed design flipflop can be implemented in any of the sequential circuits in order to analyze the efficient performance of the system. Finally, all the performance characteristics of the flipflop which includes setup time, hold time, delay, average power, clock tree power and the layout area should be compared with the existing flipflop designs.

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